REMARKS

Claims 1-36 were pending in the application. Claims 4 and 14 have been cancelled. Claims 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 23, 25-28, 30, and 35 have been amended. Claims 1-3, 5-13, and 15-36 remain pending in the application.

Objections to the Drawings:

The drawings were objected to. In a first objection, the Examiner states that the LSSD clocks and STEP clocks shown in Figure 2 are not referred to in the disclosure. Applicant respectfully disagrees, and submits that both the LSSD clocks (also shown as LSSD_CLKA and LSSD_CLKB in Figure 9) and the STEP clocks (shown in Figure 9 as the clock signals of LBST_STEP_CLKC and LBST_STEP_CLKE) are referred to in the paragraph beginning on page 10, line 6, in conjunction with Figure 9.

The drawings were also objected to because the LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and LBST_SCAN_CLKB were not referred to in the disclosure. Applicant has amended the disclosure to include reference to the LSSD_CLKA and LSSD_CLKB signals, which are the LSSD clocks discussed above. Applicant has amended Figure 9 to remove the LBST_SCAN_CLKA and LBST_SCAN_CLKB references.

Objection to the Specification:

The specification was objected to for various informalities. Applicant has amended the specification to correct these informalities.

Objection to the Claims:

Claim 35 was objected to. Applicant has amended claim 35 in accordance with the Examiner's suggestions, and therefore suggests that this objection has been overcome.

35 U.S.C. § 112 Rejections:

Claims 4, 14, and 27 were rejected under 35 U.S.C. § 112, first paragraph for failing to comply with the enablement requirement. In particular, claims 4, 14, and 27 were rejected for the use of the term "paranoid check". Claims 4 and 14 have been cancelled, therefore their rejection is believed moot. Applicant submits that the amended version of claim 27 overcomes the 35 U.S.C. § 112, first paragraph rejection.

Claim 28 was rejected under 35 U.S.C. § 112, first paragraph for failing to comply with the enablement requirement. Applicant submits that the amended version of claim 28 is in compliance with 35 U.S.C. § 112, first paragraph.

Claims 4, 14, and 27 were rejected under 35 U.S.C. § 112, second paragraph. As noted above, claims 4 and 14 have been cancelled, therefore their rejection is believed moot. Applicant submits that the amended version of claim 27 is in compliance with 35 U.S.C. § 112, second paragraph.

Claim 26 was rejected under 35 U.S.C. § 112, second paragraph. Applicant submits that the amended version of claim 26 is in compliance with 35 U.S.C. § 112, second paragraph.

35 U.S.C. § 102 and § 103 Rejections:

Claims 1-4, 7-9, 11-14, and 19-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Motika, U.S. Patent 5,982,189. Claims 25, 29, 30, and 36 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kraus, U.S. Patent 6,587,979. Applicant respectfully traverses these rejections.

Neither of the cited references anticipates the independent claims. Motika teaches a built-in stress circuit for an integrated circuit that has a frequency generator, at least one self-test circuit, a temperature regulator and a controller. The frequency generator receives a reference clock and an adjusted temperature frequency from the temperature regulator and outputs the test frequencies needed for the self-test circuits.

The self-test circuits, which are coupled to the frequency generator, receive the test frequencies and dissipate power as the self-test circuits are being used. The temperature regulator, which is coupled to the self-test circuits and the frequency generator, senses the power dissipated (i.e., the temperature), adjusts a temperature frequency corresponding to the temperature desired, and outputs the adjusted temperature frequency. The controller, which is coupled to the frequency generator, the self-test circuits, and the temperature regulator, provides the control data necessary for testing both electrical and thermal stress conditions.

Kraus teaches a flexible built-in self-test (BIST) circuit that is incorporated into an integrated circuit (IC) for testing one or random access memories or other memories embedded in an integrated circuit regardless of the number, size or test requirements of the memories. Input data from a controller that may be conveniently partitioned among components internal and external to the IC, supplies data to the BIST circuit indicating the size of the embedded memories to be tested and selecting from among several modes of BIST operation.

In contrast, independent claim 1 recites, in pertinent part,

> "A built-in self-test controller...wherein the built-in self-test controller is geographically centralized within an integrated circuit" (Emphasis added).

Independent claims 7, 11, 19, 25, and 30 recite similar combinations of features.

Motika does not teach or suggest this combination of features. In particular, Applicant can find no teaching or suggestion of a built-in self-test controller is geographically centralized within an integrated circuit as recited in independent claims 1, 11, and 19. Similarly, with respect to the Kraus reference, Applicant can find no teaching or suggestion of a memory self-test controller (claim 25) or a built-in self-test controller (claim 30) that is geographically centralized in an integrated circuit. Accordingly, Applicant submits that Motika fails to anticipate independent claims 1, 7, and 11, while

Kraus fails to anticipate independent claims 25 and 30. Accordingly, removal of the 35 U.S.C. § 102(b) rejections is respectfully requested.

Claims 5, 15, 18, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Au, U.S. Patent 6,681,359. Claims 17 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Kim, U.S. Patent 6,148.426. Claims 6, 10, 16, and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Zuraski, U.S. Patent 6,560,740, and in further view of Lo, U.S. Patent 5,661,732. Claims 26, 27, 31 and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Lo. Claims 28 and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kraus in view of Motika. Claim 34 was rejected under 35 U.S.C. § as being unpatentable over Kraus in view of Au. Claim 35 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kraus in view of Arimilli, U.S. Patent 6,665,828.

Applicant respectfully traverses these § 103(a) rejections and submits that, for at least the reasons stated above in regard to the § 102(b) rejections that the cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. Accordingly, Applicant respectfully requests removal of the 35 U.S.C. § 103(a) rejections.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-56100/BNK.

Respectfully submitted,

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